CLAIMS:

1. A method of manufacturing an electronic device, a semiconductor device in particular but not exclusively, which method comprises the steps of:
- applying a semiconductor substrate (1) which is provided with a conductor (3,4,5) at a surface (2), the conductor (3,4,5) having a top surface portion (6) and sidewall portions (7), of which at least the top surface portion (6) is provided with an etch stop layer (12),
- applying a dielectric layer (13),
- etching a via (14,15,16) in the dielectric layer (13) over the conductor (3,4,5), and stopping on the etch stop layer (12) to create an exposed part of the etch stop layer (12),
- removing the exposed part of the etch stop layer (12) inside the via (14,15,16) from at least the top surface portion (6) of the conductor (3,4,5),
- filling the via (14,15,16) with a conductive material (18)
characterized in that a layer comprising silicon carbide is applied as the etch stop layer (12).

2. A method as claimed in claim 1, characterized in that the etch stop layer is applied to the top surface portion and the sidewall portions of the conductor after the provision of the conductor at the surface of the semiconductor substrate.

3. A method as claimed in claim 2, characterized in that the via is etched while overhanging at least one of the sidewall portions of the conductor and exposing at least part of the etch stop layer, which etch stop layer covers the top surface portion and the at least one of the sidewall portions of the conductor.

4. A method as claimed in claim 3, characterized in that the etch stop layer is removed from inside the via from only the top surface portion of the conductor.

5. A method as claimed in claim 2, 3 or 4, characterized in that the etch stop layer is applied to the top surface portion and the sidewall portions of the conductor as well as to portions of the semiconductor substrate which are not covered by the conductor.

Sub. A1 Concluded

6. A method as claimed in any one of the preceding claims, characterized in that the conductor is provided while comprised at least in part of a material selected from a group comprising aluminum, copper and tungsten.

7. A method as claimed in any one of the preceding claims, characterized in that the conductor is provided comprising a capping layer, which capping layer provides the top surface portion of the conductor.

8. A method as claimed in claim 7, characterized in that the capping layer is comprised of a material selected from a group comprising titanium nitride, titanium tungsten and tantalum nitride.

Sub. A2

9. A method as claimed in any one of the preceding claims, characterized in that the dielectric layer is applied by depositing a dielectric material having a dielectric constant lower than that of silicon oxide.

10. A method as claimed in claim 9, characterized in that the dielectric layer is applied by depositing a material selected from a group comprising hydrogen silsesquioxane, parylene and a fluorinated polyimide.

Sub. A3

11. A method as claimed in any one of the preceding claims, characterized in that the via is filled by depositing a conductive layer, which conductive layer comprises a metal selected from a group comprising aluminum, copper and tungsten.

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